ZEIT2208 Programmable Digital Systems

Assignment Four

Music Synthesizer Using VHDL on an FPGA

For this assignment you will be required to write a VHDL entity to implement a music synthesizer. You will then synthesize your design on the Xilinx Spartan FPGA on the NB3000 development board. To test your design you will use your music synthesizer design to play a short sequence of notes via the speaker on the NB3000.

Pre-Lab: Complete Exercises 1 to 3 from the VHDL section of the lecture notes. Include any plots generated in the exercises, with appropriate explanations, in your pre-lab report.
(Hint: Do not cut and paste code from the lecture notes into Altium as this will cause syntax errors which are very hard to diagnose.)

Task 1: Write the following VHDL entity:

My_Music_Score

This entity should have the following inputs:

1. A clock signal.

and the following outputs:

2. A 12-bit binary number.

This entity should output a sequence of 12-bit binary numbers which correspond to the following frequencies for the musical notes of a well-known tune:

1319, 1175, 699, 699, 784, 784, 1047, 988, 587, 587, 659, 659, 988, 880, 523, 523, 659,659, 880, 880, 880, 880

The entity should output each 12-bit number for the period of the input clock signal. After the last frequency, the entity should wait for two periods of the input clock signal and then begin outputting the sequence again.

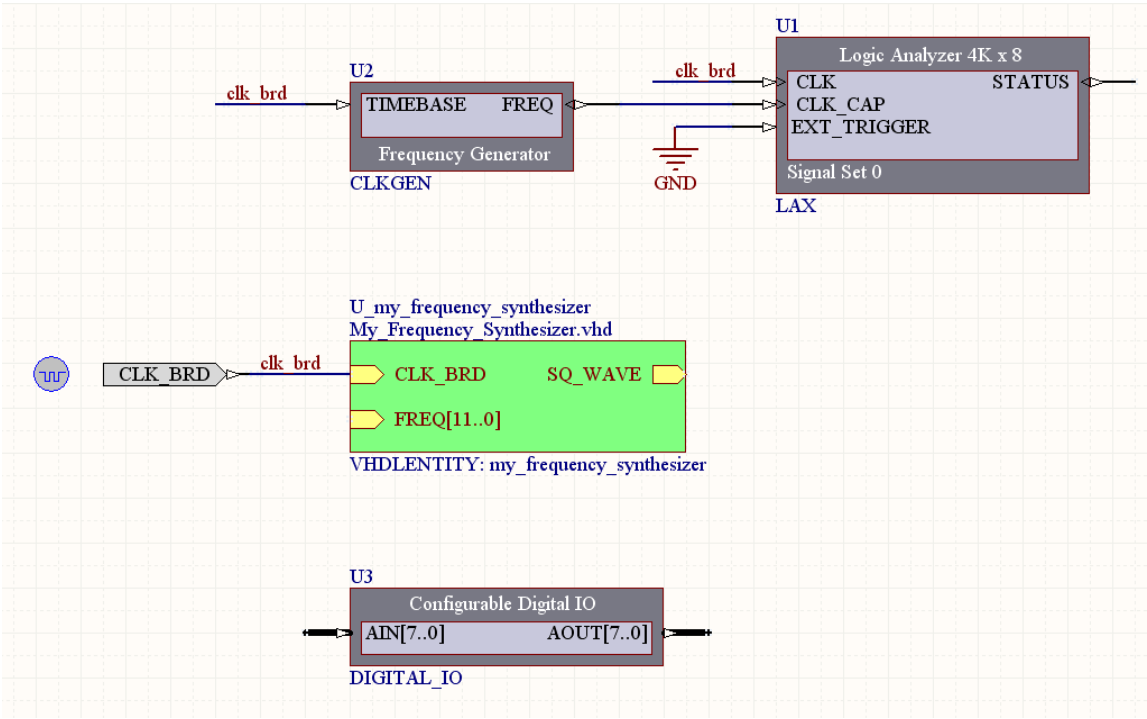
Include the final version of your VHDL code in your report. Include comments in your code to explain the function of each part of the program.

Task 2: **Frequency Synthesis**

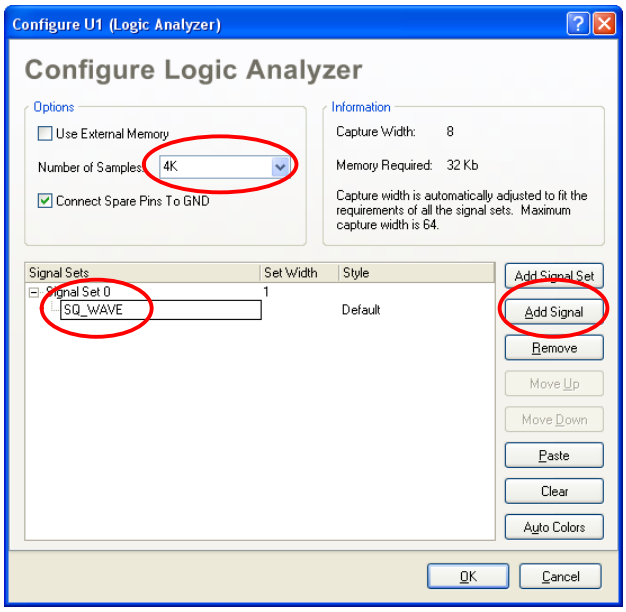
1. Create a new FPGA Project using “File>>New>>Project>>FPGA Project” and save it. Right-click on the project, and choose “Add Existing to Project>>VHDL Document” to add the VHDL file containing the My_Frequency_Synthesizer entity. This file is available on the Moodle site in the Assignment 4 section. Right-click on the project, and choose “Add New to Project>>Schematic”. Place the components shown below into your schematic and connect them as shown.

   To create a sheet symbol from your VHDL entity choose “Design>>Create Sheet Symbol From Sheet or HDL” and then select the “My_Frequency_Synthesizer.vhd” file and press OK. Place the sheet symbol and adjust the size of the sheet and the port positions as required.

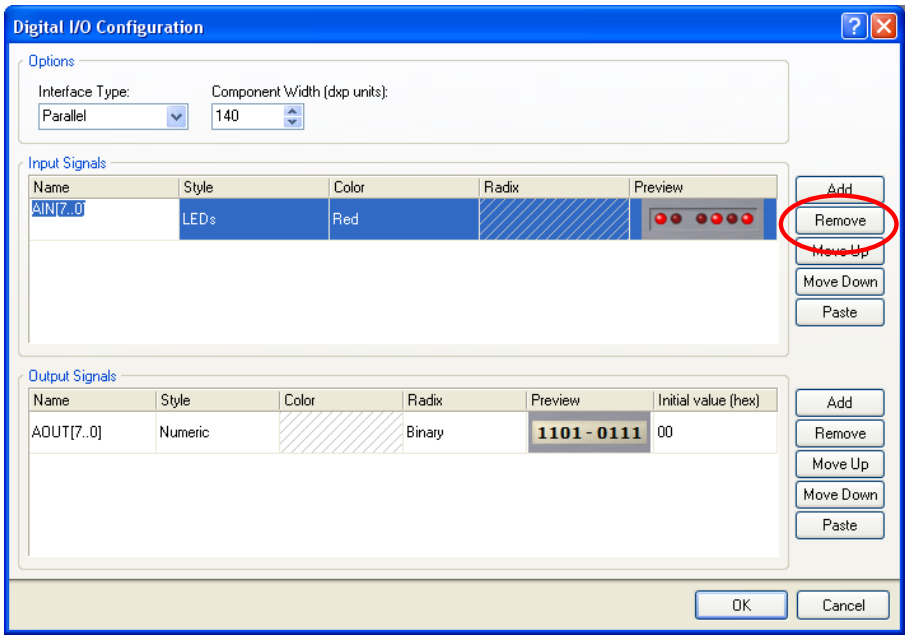
   The Logic Analyzer, Frequency Generator and Configurable Digital IO components can be found in the “FPGA Instruments” library and the CLK_BRD port component can be found in the “FPGA NB3000 Port-Plugin” library.



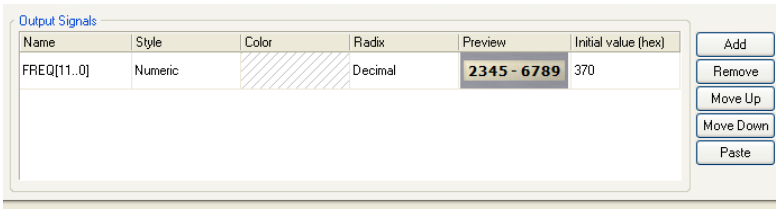
2. Next configure the logic analyzer to receive one input signal by double-clicking on the component symbol and then clicking on the “Configure…” button to bring up the dialog window shown below. Click on the “Add Signal” button and type in the name of the square wave output signal “SQ_WAVE”. Next set the number of samples to capture to 4K using the drop down box.



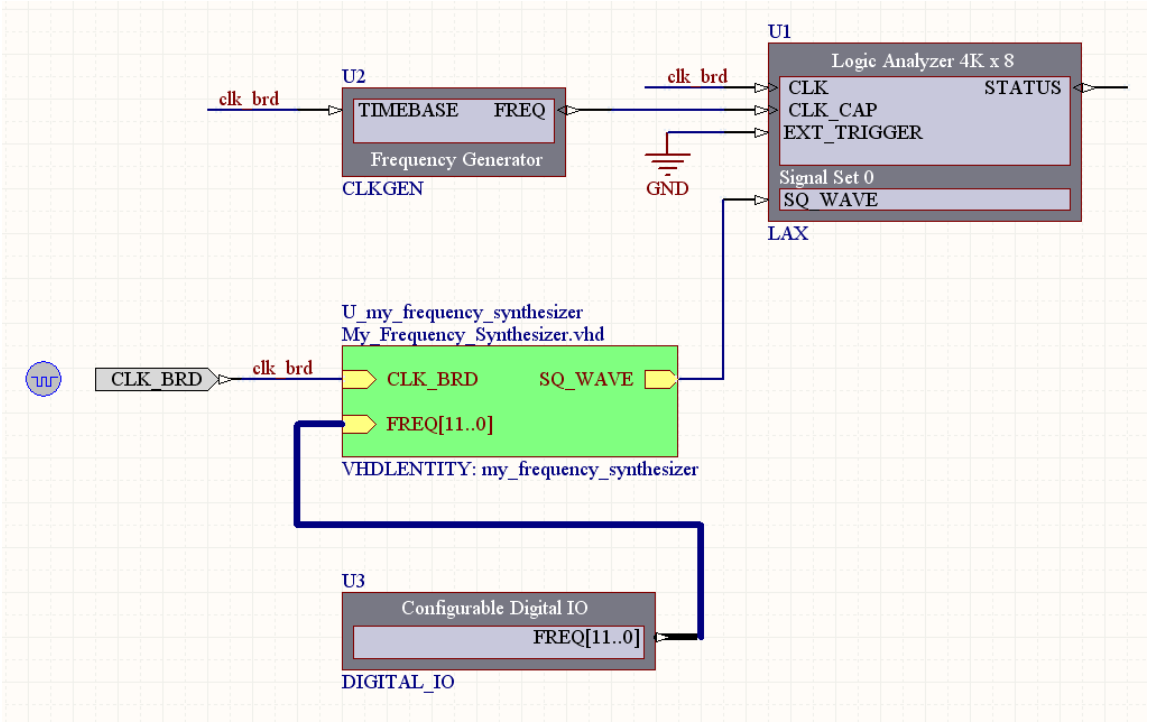
3. Now configure the Digital I/O component by double-clicking on the component symbol and then clicking on the “Configure…” button to bring up the dialog window shown below. Remove the input signals by first clicking on any of the fields to highlight the signals and then clicking the “Remove” button as shown below.



4. Configure the output signals by renaming them to FREQ[11..0], changing the radix to decimal and setting the initial value to 370 (corresponding to a frequency of 880 Hz in decimal). The output signals region of the dialogue window should now appear as shown below.

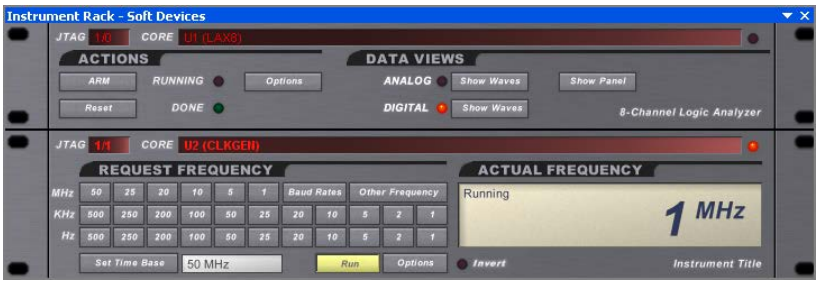


5. Now wire up the Logic Analyzer and Digital I/O components as shown below.

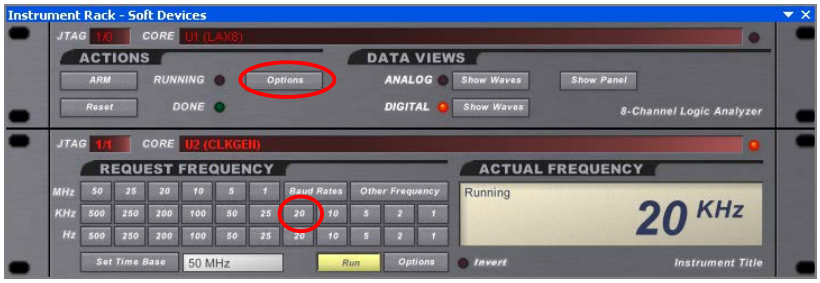


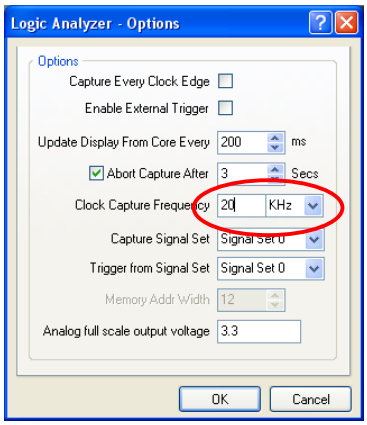
6. Target the design to the Spartan FPGA and process the design using the procedure described in Tutorial 2.

7. Once the FPGA is programmed, double-click on the icons for the Logic Analyzer and CLKGEN virtual instruments in the soft devices chain to display their associated instrument panels in the Instrument Rack – Soft Devices panel as shown below.



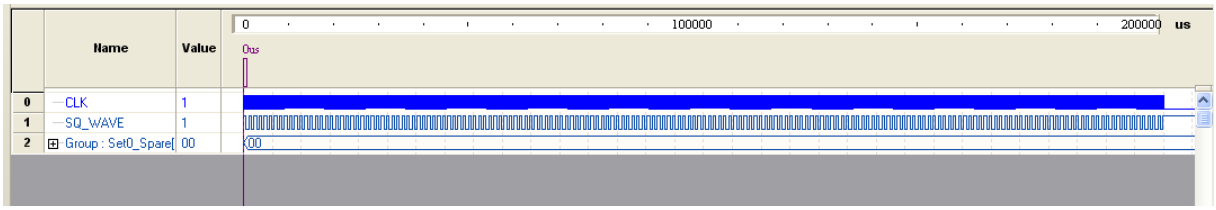
8. Change the frequency generated by the CLKGEN to 20 kHz. Open the “options” dialogue window for the Logic Analyzer and set the clock capture frequency to 20 kHz as shown below.





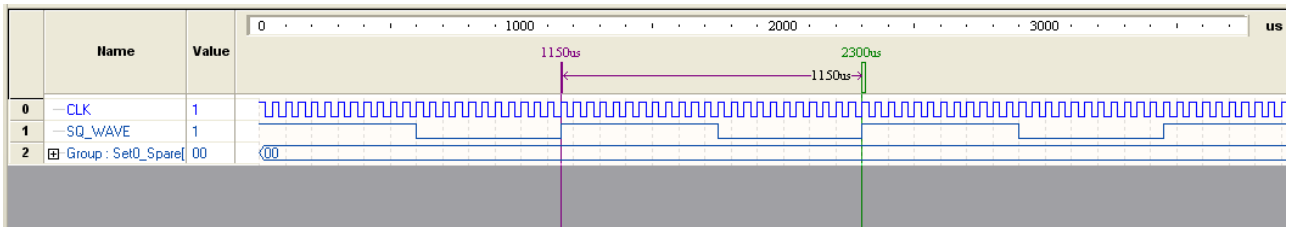
9. Now press the ARM button on the logic analyser to capture data from the SQ_WAVE output of the frequency synthesizer.

10. Close the trigger panel which is automatically displayed and observe the captured signal in the waveform editor (*.LaxDig file). It should look similar to the figure below.



11. Add an extra measurement cursor to the waveform editor using “Edit>>Set Cursor>>Add New Cursor”. You can move them by clicking on their “handles” above the waveform display (below the time ruler at the top).

12. Zoom in on the waveforms using CTRL+Mouse Scroll Wheel and move the cursors around to measure the period of the square wave produced by your frequency synthesizer as shown below.

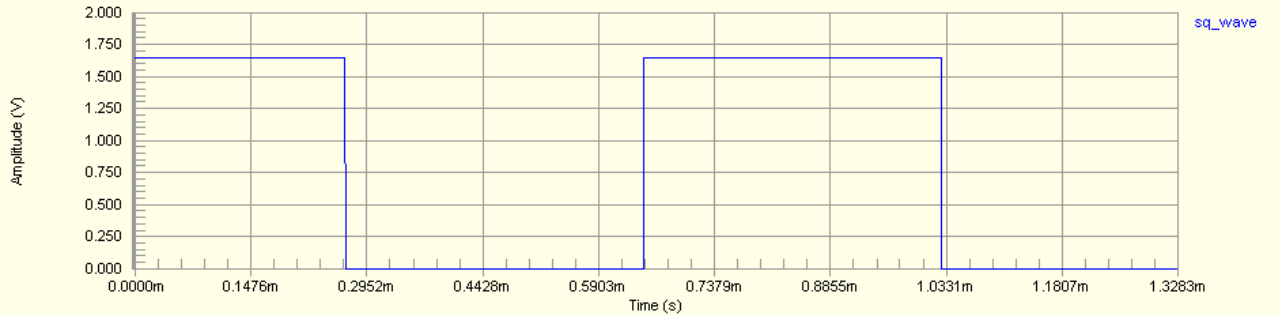


13. Calculate the estimated frequency of the square wave output of your frequency synthesizer using the period measured in the previous step.

14. Repeat steps 8 to 13 for capture frequencies of 100 kHz and 1 MHz in the Logic Analyzer instrument. (Remember to change the frequency in both the CLKGEN instrument and the Options dialogue of the Logic Analyzer instrument.)

15. Explain why the estimated frequencies for your square wave using these two capture frequencies are different. Which capture frequency is the best to use? Why?

16. Press the “Show Waves” button for the “ANALOG” data view on the Logic Analyzer instrument panel and press the ARM button to capture both an analog and digital view of the waveform. Switch to the analog view (*.LaxAn file) in the waveform editor and create a plot similar to that shown below for the square wave output from your frequency synthesizer. Include this plot in your report.

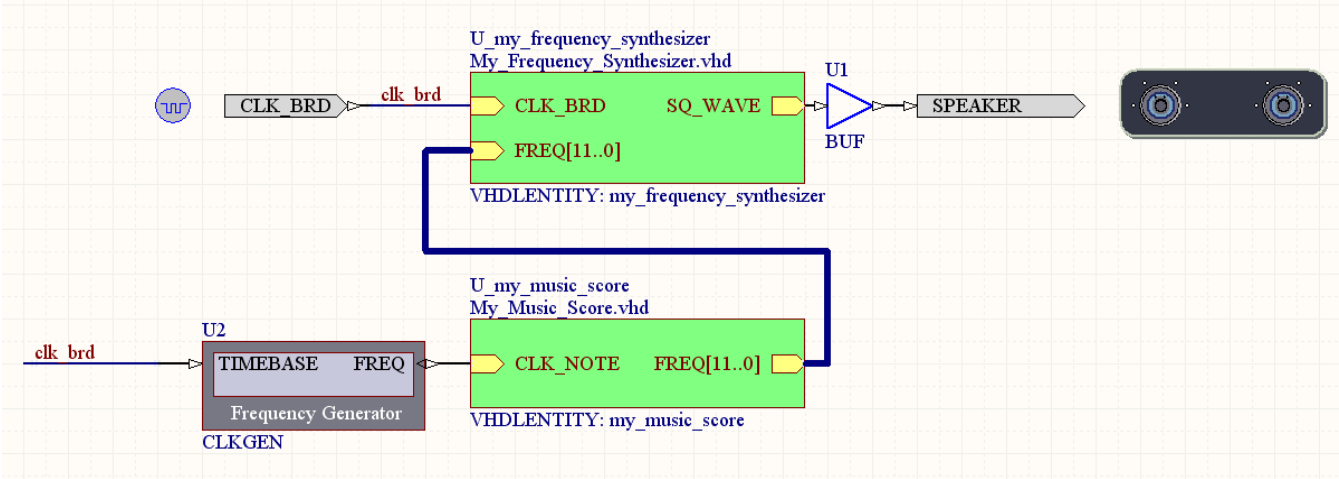


17. Double-click on the Digital I/O icon virtual instrument in the soft devices chain to display its instrument panel in the Instrument Rack. Change the output frequency of the frequency synthesizer by typing in a new frequency and pressing the double-arrow button as shown below.

18. Test the frequency synthesizer to verify that it produces square waves at all frequencies within the required range.

Task 3: **Playing a Music Score**

1. Now replace the Digital I/O instrument with your My_Music_Score VHDL entity and a frequency generator instrument. Connect the output of your frequency synthesizer to the speakers on the Nanoboard via a buffer as shown below. The BUF component can be found in the "FPGA Generic" Library and the SPEAKER component can be found in the "FPGA NB3000 Port-Plugin" library.



2. Program the FPGA and display the CLKGEN instrument panel. Set the frequency to 5 Hz and verify that the tune is being played continuously through the Nanoboard speakers. (Don't forget to increase the volume using the volume knob shown below)

3. Explain the operation of this circuit and describe the effect of changing the frequency using the CLKGEN instrument panel.

Useful References: The following are useful documents provided by Altium in your installations that describe the components in more detail. See the help menu in Altium of your installation directory Help folder.

CR0100 CLKGEN Frequency Generator.
CR0118 FPGA Generic Library Guide.
CR0158 LAX Configurable Logic Analyzer.
CR0179 DIGITAL_IO Configurable Digital IO Module.